Description

The μPD70116 (V30) is a CMOS 16-bit microprocessor with an internal 16-bit architecture and a 16-bit external data bus. The μPD70116 instruction set is a superset of the μPD8086/8088; however, mnemonics and execution times are different. The μPD70116 additionally has a powerful instruction set including bit processing, packed BCD operations, and high-speed multiplication/division operations. The μPD70116 can also execute the entire 8080 instruction set and comes with a standby mode that significantly reduces power consumption. It is software-compatible with the μPD70108 microprocessor.

Features

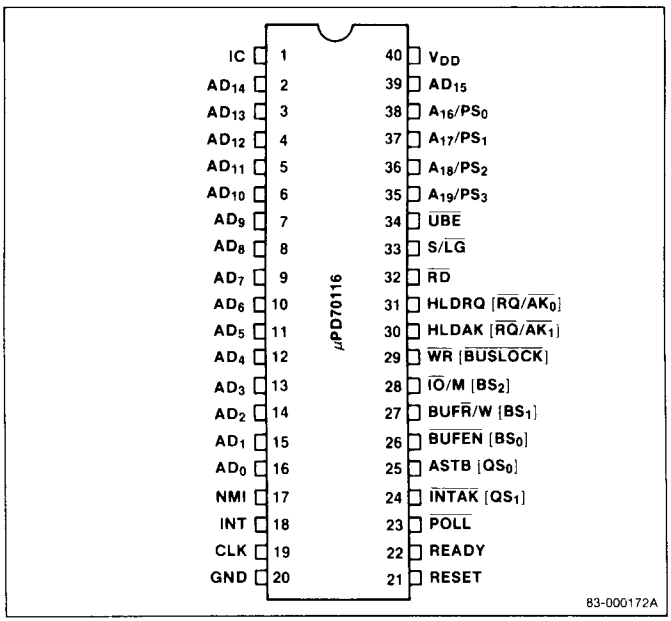
- ☐ Minimum instruction execution time: 250 ns (at 8 MHz)
- ☐ Maximum addressable memory: 1 Mbyte
- ☐ Abundant memory addressing modes
- ☐ 14 x 16-bit register set
- ☐ 101 instructions
- ☐ Instruction set is a superset of μPD8086/8088 instruction set
- ☐ Bit, byte, word, and block operations
- ☐ Bit field operation instructions
- ☐ Packed BCD instructions
- ☐ Multiplication/division instruction execution time: 4 μs to 6 μs (at 8 MHz)
- ☐ High-speed block transfer instructions: 2 Mbyte/s (at 8 MHz)
- ☐ High-speed calculation of effective addresses: 2 clock cycles in any addressing mode
- ☐ Maskable (INT) and nonmaskable (NMI) interrupt inputs
- ☐ IEEE-796 bus compatible interface
- ☐ 8080 emulation mode
- ☐ CMOS technology
- ☐ Low-power consumption
- ☐ Low-power standby mode
- ☐ Single power supply
- ☐ 5-MHz, 8-MHz or 10-MHz clock

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD70116C-5	40-pin plastic DIP	5 MHz
μPD70116C-8	40-pin plastic DIP	8 MHz
μPD70116D-5	40-pin ceramic DIP	5 MHz
μPD70116D-8	40-pin ceramic DIP	8 MHz
μPD70116D-10	40-pin ceramic DIP	10 MHz
μPD70116G-5	52-pin flat pack	5 MHz
μPD70116G-8	52-pin flat pack	8 MHz
μPD70116L-5	44-pin PLCC	5 MHz
μPD70116L-8	44-pin PLCC	8 MHz

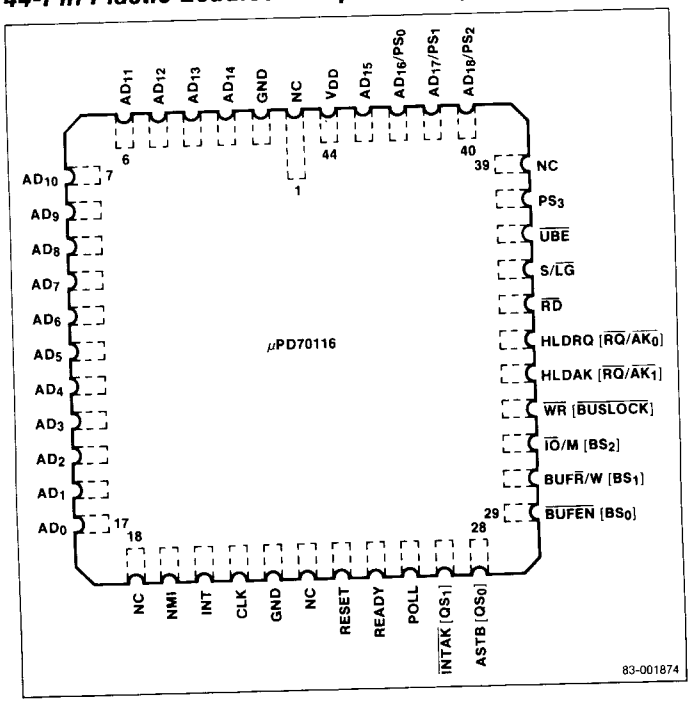
Pin Configurations

40-Pin Plastic DIP/Cerdip

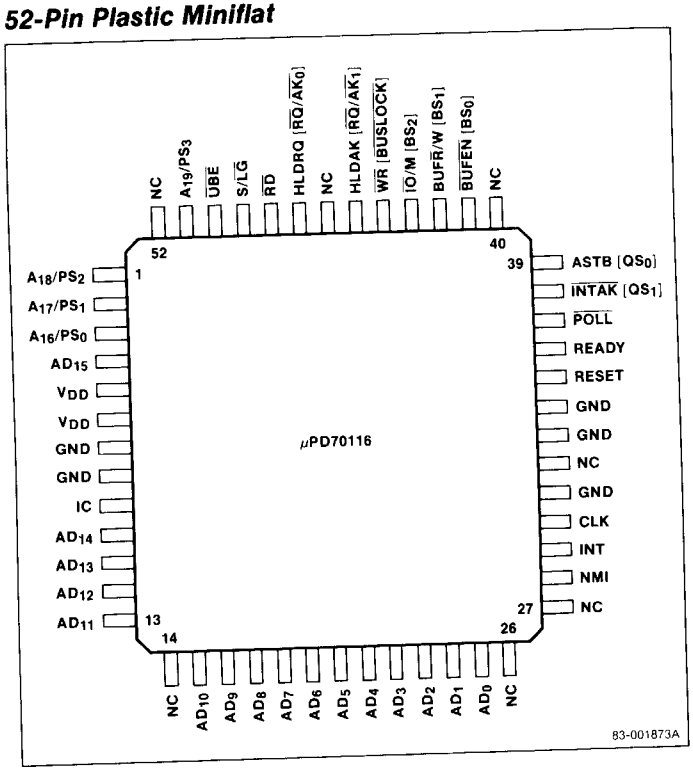


Pin Configurations (cont)

44-Pin Plastic Leadless Chip Carrier (PLCC)



52-Pin Plastic Miniflat



Pin Identification

No.	Symbol	Direction	Function
1	IC*		Internally connected
2 - 16	AD_{14} - AD_0	In/Out	Address/data bus
17	NMI	In	Nonmaskable interrupt input
18	INT	In	Maskable interrupt input
19	CLK	In	Clock input
20	GND		Ground potential
21	RESET	In	Reset input
22	READY	In	Ready input
23	$\overline{POLL}$	In	Poll input
24	$\overline{INTAK}$ (QS_1)	Out	Interrupt acknowledge output (queue status bit 1 output)
25	ASTB (QS_0)	Out	Address strobe output (queue status bit 0 output)
26	$\overline{BUFEN}$ (BS_0)	Out	Buffer enable output (bus status bit 0 output)
27	$BUF\overline{R}/W$ (BS_1)	Out	Buffer read/write output (bus status bit 1 output)
28	$\overline{IO}/M$ (BS_2)	Out	Access is I/O or memory (bus status bit 2 output)
29	$\overline{WR}$ ($\overline{BUSLOCK}$)	Out	Write strobe output (bus lock output)
30	HLDAK ($\overline{RQ}/\overline{AK_1}$)	Out (In/Out)	Hold acknowledge output, (bus hold request input/ acknowledge output 1)
31	HLDRQ ($\overline{RQ}/\overline{AK_0}$)	In (In/Out)	Hold request input (bus hold request input/ acknowledge output 0)
32	$\overline{RD}$	Out	Read strobe output
33	$S/\overline{LG}$	In	Small-scale/large-scale system input
34	$\overline{UBE}$	Out	Upper byte enable
35 - 38	A_{19}/PS_3 - A_{16}/PS_0	Out	Address bus, high bits or processor status output
39	AD_{15}	In/Out	Address/data bus, bit 15
40	V_{DD}		Power supply

Notes: * IC should be connected to ground.

Where pins have different functions in small- and large-scale systems, the large-scale system pin symbol and function are in parentheses.

Unused input pins should be tied to ground or V_{DD} to minimize power dissipation and prevent the flow of potentially harmful currents.

Block Diagram